Abstracts

High gain, high efficiency, low voltage, medium power Si-bipolar transistor suitable for integration

F. van Rijs, R. Dekker, P.H.C. Magnee, R. Vanoppen, E. v.d. Heijden, B.N. Balm and L.C. Colussi. "High gain, high efficiency, low voltage, medium power Si-bipolar transistor suitable for integration." 1997 Radio Frequency Integrated Circuits (RFIC) Symposium 97. (1997 [RFIC]): 15-18.

Medium power transistors in a high performance double polysilicon bipolar process have been fabricated. On-wafer loadpull measurements show high gain (15 dB) and high maximum efficiency (60%) at 1.8 GHz with 27 dBm of output power. These results were obtained with a low supply voltage of 3.5 V. More importantly, these results were obtained with transistors with a buried layer having a collector contact at the top, which makes it possible to integrate power amplifiers on chip.

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